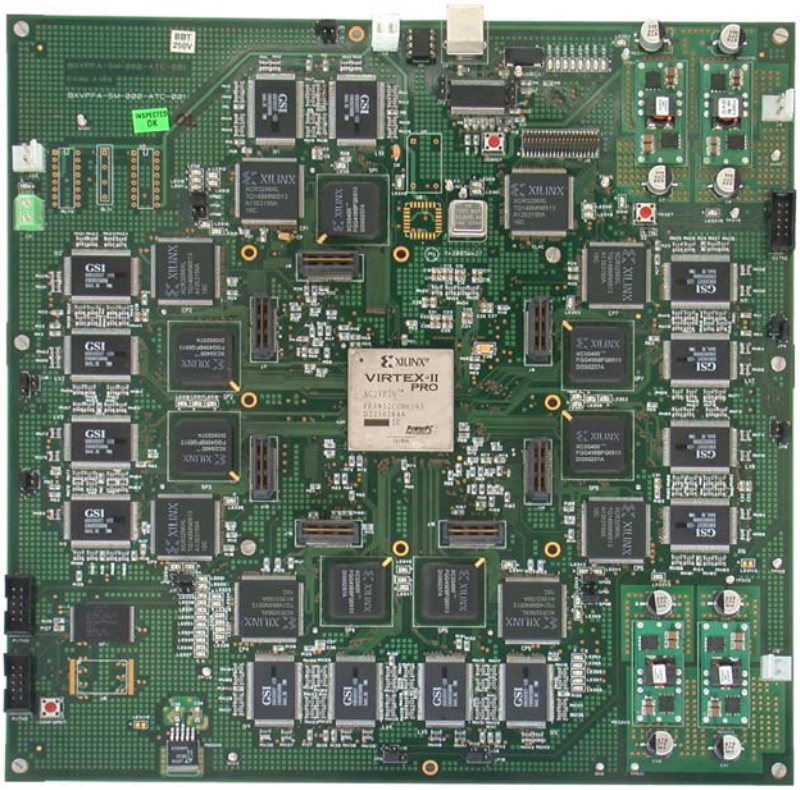
Photo of the entire system



Overview

This board is an ASIC tester used to test ASIC prototypes. We provide a hardware test environment to functionally test ASIC prototypes. Highlight of our approach is the reuse of test benches that have already been developed and used during the ASIC design cycle. This result in a saving, in terms of testing time, testing effort and therefore testing cost. We have designed an FPGA based hardware and a set of software tools. The software tools pre process a test bench and download it into the FPGA, which is further applied in real time to the ASIC under test (DUT). Results from the DUT are logged in real time and the software tool converts these results to a VCD (Value Change Dump) file format, which can be viewed in a standard simulation tool as waveforms. The test/design engineer can then analyze these waveforms (similar to what he did during his design verification phase). Thus our ASIC tester closes the gap between simulation and real hardware testing.

Features

The project has been divided into 3 parts, viz. Hardware, Software and Test Patterns.

Hardware:

Symmetrically designed system consisting of

1. Virtex 2 Pro FPGA as a master controller.
2. 7 Spartan 3 FPGAs as 7 different slave controllers.
3. 224 Configurable I/Os (5V Tolerant).
4. Storage capacity of 1M input test samples.
5. Storage capacity of 1M logged samples.
6. USB interface to upload/download Test Patterns.
7. On board power supply.

Software:

1. User friendly GUI.
2. Upload/Download Test patterns to/from ASIC tester using PCs USB port.

PCB Specifications

1. Twelve layer board: Seven signal planes and five power planes.
2. Termination resistors for signal integrity issue.
3. High speed/High density (0.5 mm pitch) headers.
4. Length matching of tracks for high speed issues.

Customer Requirements

1. Primary Application – Testing of ASIC Prototypes.
2. Type of ASIC – Digital only (5V Tolerant).
3. Type of test – Minimal Functional.
4. Set up time – As low as possible.
5. Length of test – As large as possible.
6. Capacity – Should be able to test ASICs with up to 224 I/Os.
7. ASIC Clock – Maximum 10 MHz.
8. Test Pattern Speed – Anything above 50 MHz.
9. Ability to handle bi directional buses.